

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

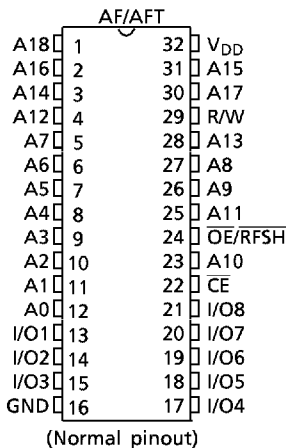
The TC51V8512AF/AFT is a 4,194,304-bit CMOS pseudo static random access memory (PSRAM) organized as 524,288 words by 8 bits. It features a one-transistor dynamic memory cell using CMOS peripheral circuitry to provide large capacity, high speed and low power. It uses a single 2.7 to 3.6 V power supply. An OE/RFSH input selects either auto or self refresh operation. This device family also features SRAM-like write functions whereby data is written to the memory cell rising edge of R/W signal, for easy interfacing to microprocessors. The TC51V8512AF/AFT is molded in 32-pin 0.525-inch small-outline plastic packages (SOP), and thin small-outline plastic package (TSOP).

FEATURES

- Organized as 524,288 words by 8 bits (4,194,304 bits).
- Fast access time and low power dissipation.
- Single power supply voltage of 2.7 to 3.6 V.
- Data retention power supply voltage of 2.0 to 3.6 V.
- Internal counter can be used for auto and self refresh operations.
- Internal timer can be used for self refresh operation.
- 2048 refresh cycles per 32 ms.
- All inputs and outputs are TTL compatible.
- Logic compatible with SRAM R/W pin.
- Packages:
 - SOP32-P-525-1.27 (AF) (Weight: 1.10 g typ)
 - TSOP II 32-P-400-1.27 (AFT) (Weight: 0.51 g typ)

	TC51V8512AF Family	
	-12	-15
t_{CEA} \overline{CE} Access Time	120 ns	150 ns
t_{OEA} \overline{OE} Access Time	60 ns	80 ns
t_{RC} Cycle Time	190 ns	230 ns
Power Dissipation	99 mW	66 mW
Self Refresh Current	3.0 V 40 μ A	

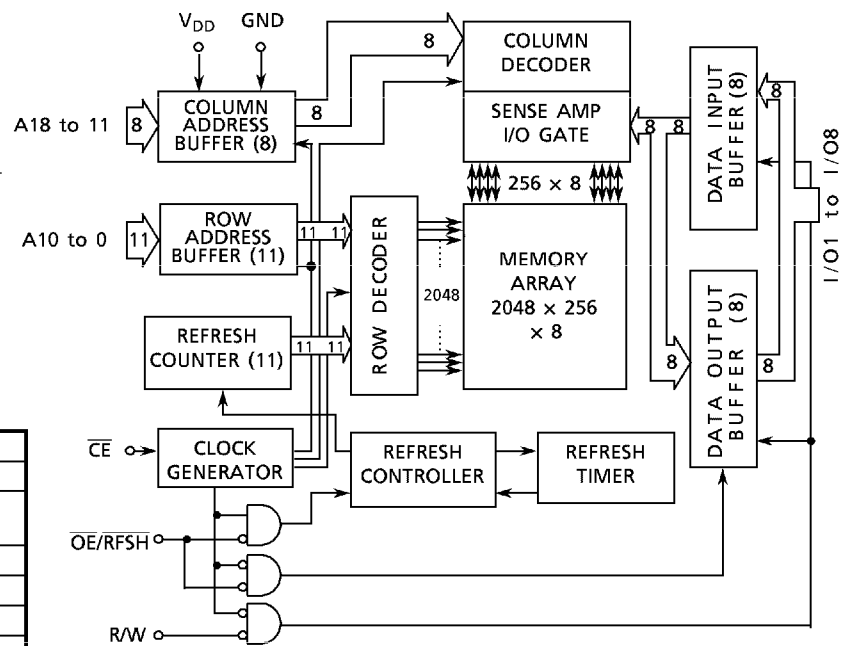
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

Pin	Name
A0 to A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}/RFSH$	Output Enable Refresh Input
\overline{CE}	Chip Enable
I/O1 to I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



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TRUTH TABLE

CE	OE/RFSH	R/W	A0 to A18	I/O1 to 8	CONDITION
L	L	x	x x	OUT	Read
L	x	x	x x	IN	Write
L	H	x	x x	HZ	CE Only Refresh
H	L	x	x	HZ	Auto/Self Refresh
H	H	x	x	HZ	Stand by

- H ... High Level Input ($V_{IN} = 6.0\text{ V to }V_{IH}\text{ min}$)
- L ... Low Level Input ($V_{IN} = V_{IL}\text{ max to }-0.5\text{ V}$)
- X ... Don't care
- XX ... At CE falling edge, all address are "IN", and at the other condition, the address are "X"
- HZ ... High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT	NOTE
V_{IN}	Input Voltage	- 1.0 to 7.0	V	1
V_{OUT}	Output Voltage	- 1.0 to 7.0	V	
V_{DD}	Power Supply Voltage	- 1.0 to 7.0	V	
T_{OPR}	Operating Temperature	0 to 70	°C	
T_{STG}	Storage Temperature	- 55 to 150	°C	
T_{SOLDER}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ\text{ to }70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{DD}	Power Supply Voltage	2.7	3.0	3.6	V	2
V_{IH}	Input High Voltage	2.1	-	6.0	V	2
V_{IL}	Input Low Voltage	- 0.5	-	0.4	V	2

DC CHARACTERISTICS ($V_{DD} = 3\text{ V} \pm 10\%$, $T_a = 0^\circ$ to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE	
I _{DDO}	Operating Current (Average Power Supply) \overline{CE} , Address Cycling: $t_{RC} = t_{RC\text{ min}}$	120 ns version	-	20	30	mA	3, 4
		150 ns version	-	15	20		
I _{DD51}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IH}$	-	-	0.5	mA		
I _{DD52}	Standby Current $\overline{CE} = V_{DD} - 0.2\text{ V}$, $\overline{OE/RFSH} = V_{DD} - 0.2\text{ V}$	-	-	40	μA		
I _{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IL}$	-	-	0.5	mA		
I _{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2\text{ V}$, $\overline{OE/RFSH} = 0.2\text{ V}$	-	-	40	μA		
I _{DDF3}	Auto Refresh Current (Average) ($\overline{OE/RFSH}$ Cycling: $t_{FC} = t_{FC\text{ min}}$)	120 ns version	-	20	30	mA	3
		150 ns version	-	15	20		
I _{DDF4}	\overline{CE} Only Refresh Current (Average) (\overline{CE} , Address Cycling: $t_{RC} = t_{RC\text{ min}}$)	120 ns version	-	20	30	mA	3
		150 ns version	-	15	20		
I _{I(L)}	Input Leakage Current $0\text{ V} \leq V_{IN} \leq V_{DD}$, All Other Inputs Not Under Test = 0 V	- 10	-	10	μA		
I _{O(L)}	Output Leakage Current Output Disable ($\overline{CE} = V_{IH}$ or $\overline{OE/RFSH} = V_{IH}$ or $R/W = V_{IL}$), $0\text{ V} \leq V_{OUT} \leq V_{DD}$	- 10	-	10	μA		
V _{OH}	Output High Level $I_{OH} = -100\ \mu\text{A}$	$V_{DD} - 0.2$	-	-	V		
V _{OL}	Output Low Level $I_{OL} = 100\ \mu\text{A}$	-	-	0.2	V		

CAPACITANCE ($V_{DD} = 3\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C _{I1}	Input Capacitance (A0 to A18)	-	5	pF
C _{I2}	Input Capacitance (\overline{CE} , $\overline{OE/RFSH}$, R/W)	-	7	pF
C _{I0}	Input/Output Capacitance	-	7	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($V_{DD} = 3.3 \pm 0.3 \text{ V}$, $T_a = 0^\circ \text{ to } 70^\circ \text{C}$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE	
I _{DDO}	Operating Current (Average Power Supply) \overline{CE} , Address Cycling: $t_{RC} = t_{RC \text{ min}}$	120 ns version	-	25	40	mA	3, 4
		150 ns version	-	20	30		
I _{DD51}	Standby Current $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IH}$	-	-	0.5	mA		
I _{DD52}	Standby Current $\overline{CE} = V_{DD} - 0.2 \text{ V}$, $\overline{OE/RFSH} = V_{DD} - 0.2 \text{ V}$	-	-	50	μA		
I _{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{OE/RFSH} = V_{IL}$	-	-	0.5	mA		
I _{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2 \text{ V}$, $\overline{OE/RFSH} = 0.2 \text{ V}$	-	-	50	μA		
I _{DDF3}	Auto Refresh Current (Average) ($\overline{OE/RFSH}$ Cycling: $t_{FC} = t_{FC \text{ min}}$)	120 ns version	-	25	40	mA	3
		150 ns version	-	20	30		
I _{DDF4}	\overline{CE} Only Refresh Current (Average) (\overline{CE} , Address Cycling: $t_{RC} = t_{RC \text{ min}}$)	120 ns version	-	25	40	mA	3
		150 ns version	-	20	30		
I _{I(L)}	Input Leakage Current $0 \text{ V} \leq V_{IN} \leq V_{DD}$, All Other Inputs Not Under Test = 0 V	- 10	-	10	μA		
I _{O(L)}	Output Leakage Current Output Disable ($\overline{CE} = V_{IH}$ or $\overline{OE/RFSH} = V_{IH}$ or $R/W = V_{IL}$), $0 \text{ V} \leq V_{OUT} \leq V_{DD}$	- 10	-	10	μA		
V _{OH}	Output High Level $I_{OH} = - 100 \mu\text{A}$	V_{DD} - 0.2	-	-	V		
V _{OL}	Output Low Level $I_{OL} = 100 \mu\text{A}$	-	-	0.2	V		

AC CHARACTERISTICS ($V_{DD} = 2.7$ to 3.6 V, $T_a = 0^\circ$ to 70°C) (Notes: 5, 6)

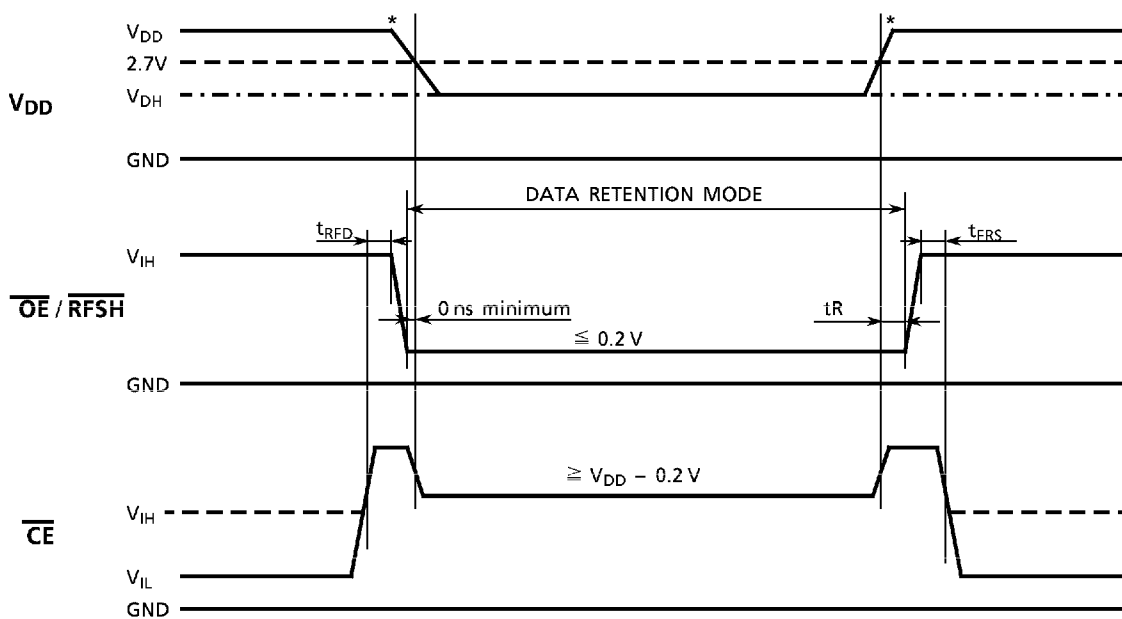
SYMBOL	PARAMETER	-120		-150		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	190	–	230	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	250	–	290	–	ns	
t_{CE}	\overline{CE} Pulse Width	120	10,000	150	10,000	ns	
t_p	\overline{CE} Precharge Time	70	–	80	–	ns	
t_{CEA}	\overline{CE} Access Time	–	120	–	150	ns	
t_{OEA}	\overline{OE} Access Time	–	60	–	80	ns	
t_{CLZ}	\overline{CE} to Output in Low-Z	20	–	20	–	ns	
t_{OLZ}	\overline{OE} to Output in Low-Z	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	5	–	5	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	30	0	30	ns	7
t_{OHZ}	\overline{OE} Disable to Output in High-Z	0	30	0	30	ns	7
t_{WHZ}	Write Enable to Output in High-Z	0	30	0	30	ns	7
t_{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	0	–	0	–	ns	7
t_{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	15	–	15	–	ns	7
t_{RCS}	Read Command Setup Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	
t_{WP}	Write Pulse Width	35	–	35	–	ns	
t_{WCH}	Write Command Hold Time	70	–	70	–	ns	
t_{CWL}	Write Command to \overline{CE} Lead Time	35	–	35	–	ns	
t_{DSW}	Data Setup Time from R/W	30	–	30	–	ns	8
t_{DSC}	Data Setup Time from \overline{CE}	30	–	30	–	ns	8
t_{DHW}	Data Hold Time from R/W	0	–	0	–	ns	8
t_{DHC}	Data Hold Time from \overline{CE}	0	–	0	–	ns	8
t_{ASC}	Address Setup Time	0	–	0	–	ns	9
t_{AHC}	Address Hold Time	25	–	25	–	ns	9
t_{FC}	Auto Refresh Cycle Time	190	–	230	–	ns	
t_{RFD}	\overline{RFSH} Delay Time from \overline{CE}	70	–	80	–	ns	
t_{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	80	8,000	80	8,000	ns	10
t_{FP}	\overline{RFSH} Precharge Time	40	–	40	–	ns	10
t_{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	–	8,000	–	ns	10
t_{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	250	–	300	–	ns	10
t_{REF}	Refresh Period (2048 cycles, A0 to A10)	–	32	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

Notes:

- 1) Stresses greater than those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device.
- 2) All voltage are referenced to GND.
- 3) I_{DDO} , I_{DDF3} and I_{DDF4} depend on cycle rate.
- 4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
- 5) An initial pause of 100 μ s with \overline{CE} High is required after power-up before proper device operation is achieved.
- 6) Measured with a load equivalent to 1 TTL load and 100 pF.
- 7) Parameters t_{CHZ} , t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 8) In write cycles, input data is latched at the earlier of the R/W or \overline{CE} rising edge. Therefore, input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 9) All address inputs are latched on the falling edge of \overline{CE} . Therefore, all address inputs must be valid during t_{ASC} and t_{AHC} .
- 10) Two refresh operations—auto refresh and self refresh—are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 - Auto refresh: \overline{RFSH} pulse width $\leq t_{FAP}(\max)$
 - Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}(\min)$The timing parameter (t_{FRS}) must be observed for proper device operation in accordance with the following conditions.
 - After self refresh
 - When $\overline{OE}/\overline{RFSH} = \text{“L”}$ after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	-	3.6	V
I _{DDF2}	Self Refresh Current	V _{DH} = 3.3 V	-	40	μA
		V _{DH} = 3.6 V	-	50	μA
t _R	Recovery Time	5	-	-	ms



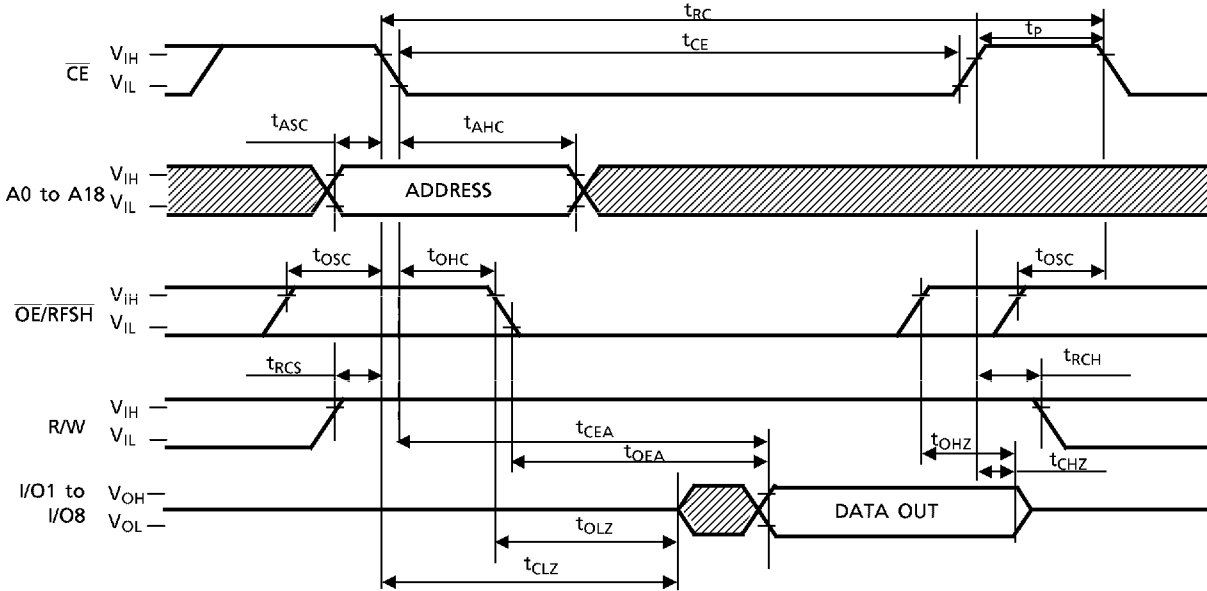
(Note)° R/W, A0 to A18 = Don't care.

- I_{DDF1} is applied with OE/RFSH = V_{IL} max, CE = V_{IH} min
- In all states except Data Retention Mode, Auto Refresh or CE-Only Refresh with 2048 cycles per 32 ms is required.

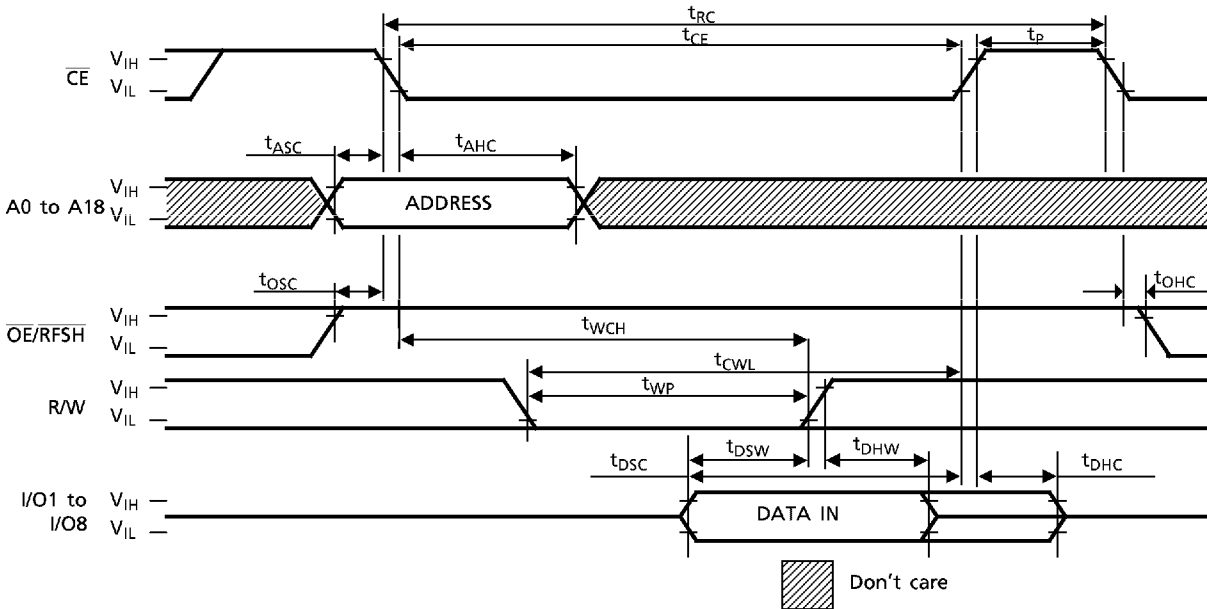
* The raising and falling slope of V_{DD} should be more than 50 ms in order to operate the device safely (20 ms/V).

TIMING DIAGRAMS

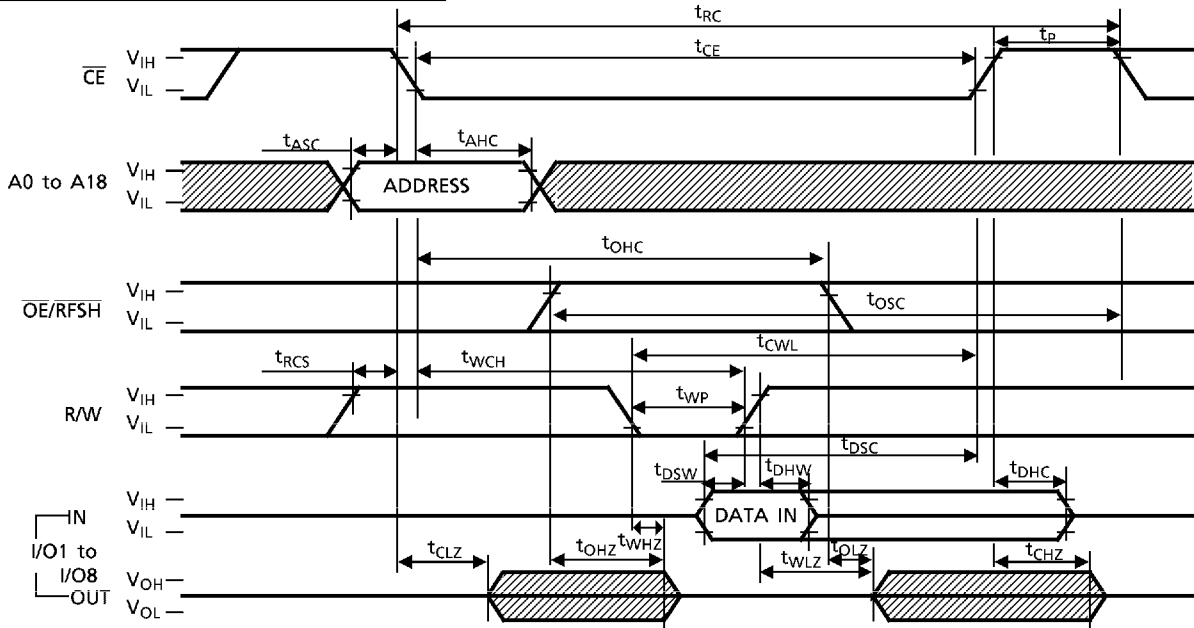
READ CYCLE



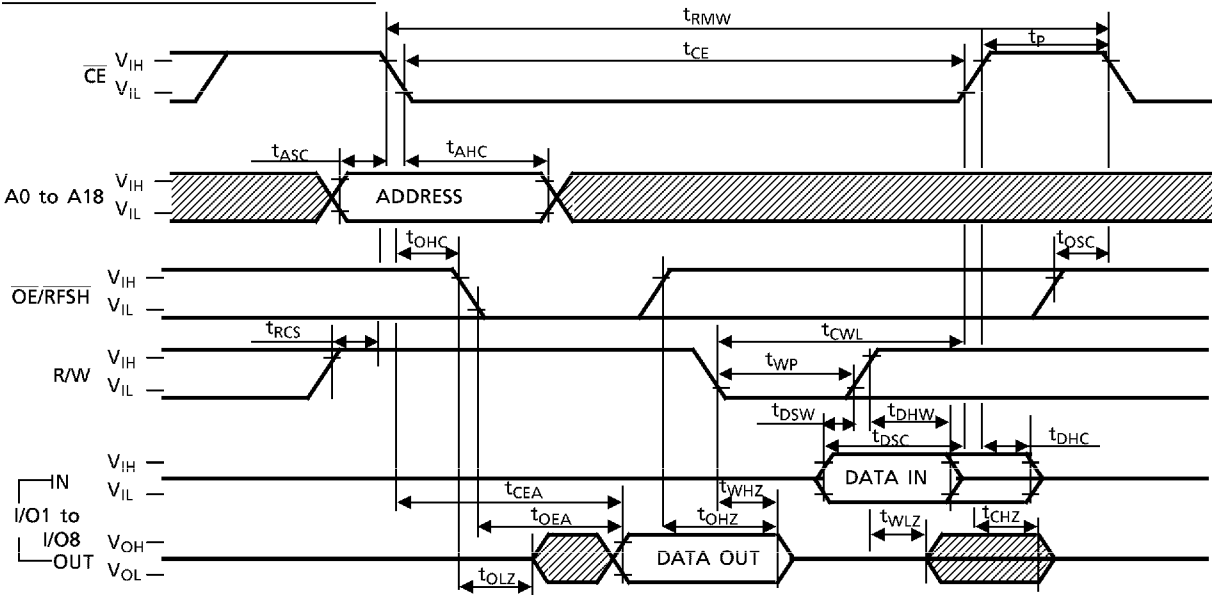
WRITE CYCLE 1 (\overline{OE} HIGH)



WRITE CYCLE 2 (\overline{OE} CLOCKED & LOW)

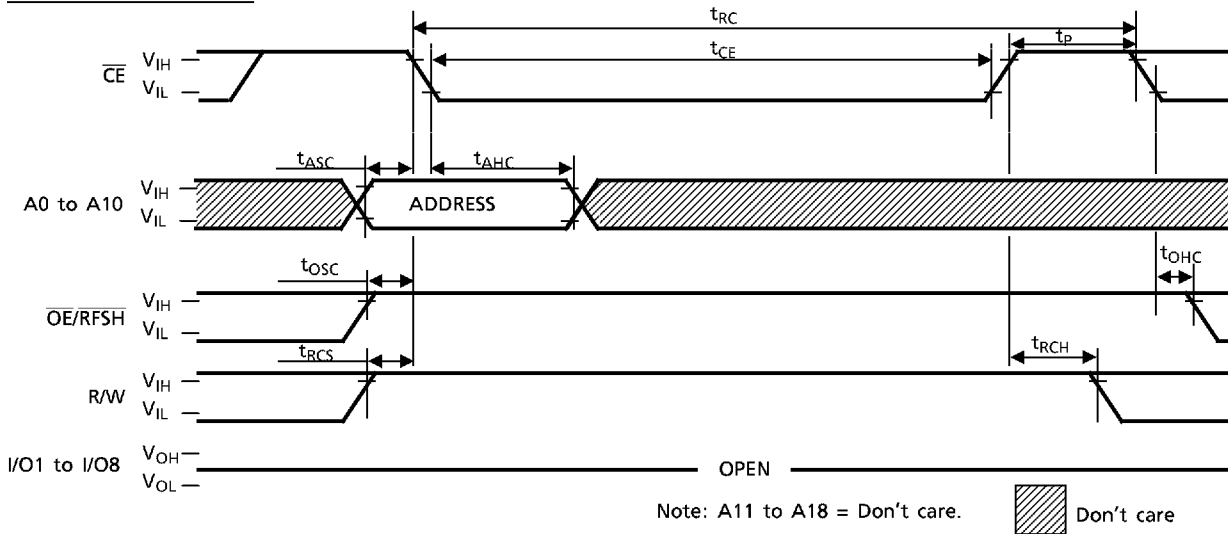


READ-MODIFY-WRITE CYCLE

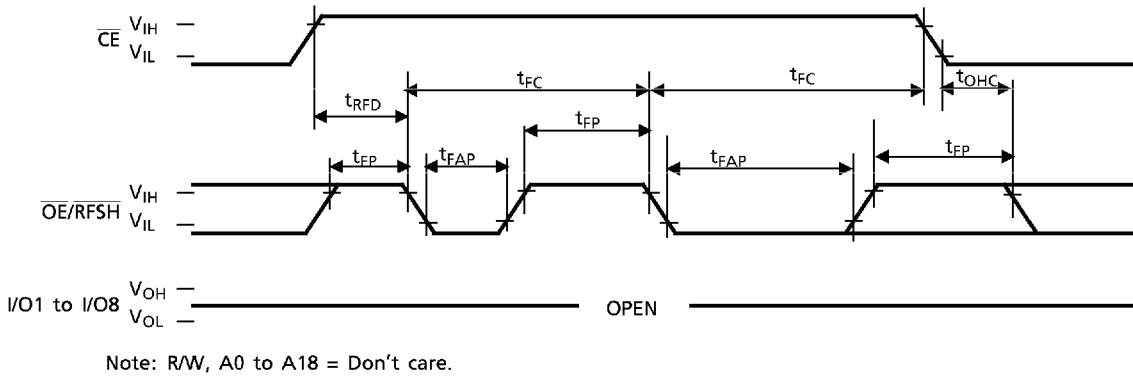


 Don't care

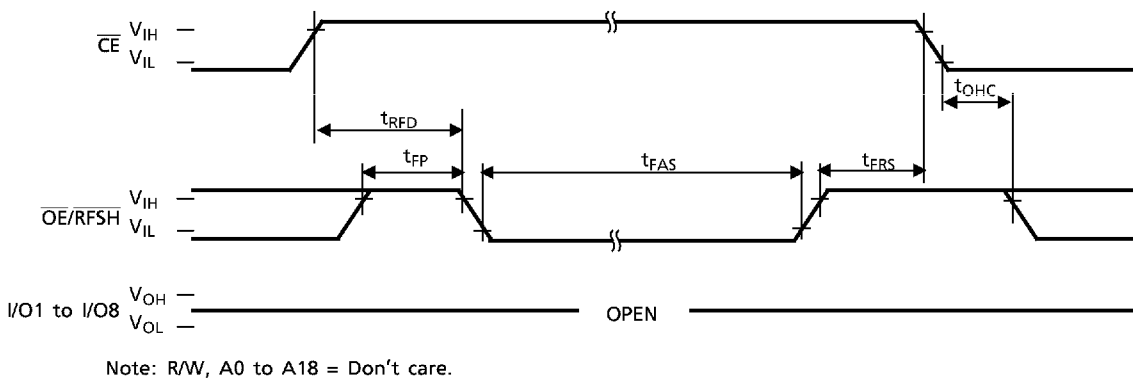
CE-ONLY REFRESH



AUTO REFRESH

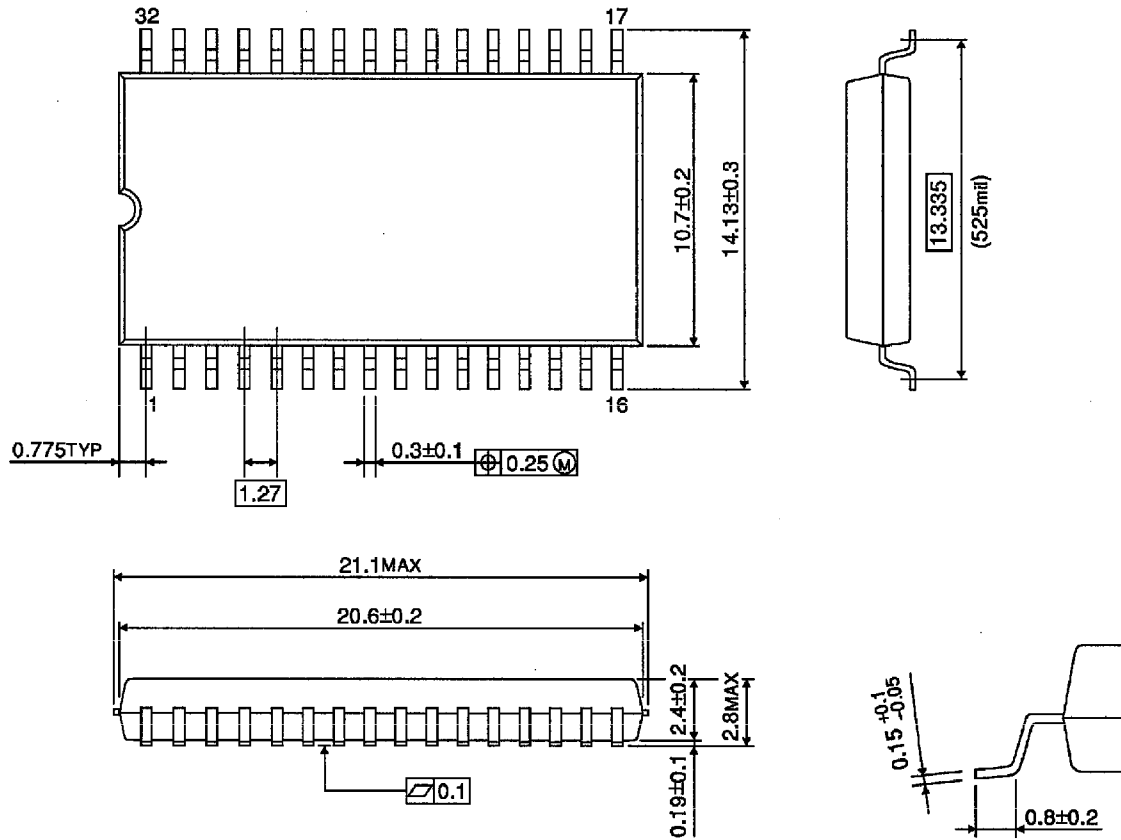


SELF REFRESH



PACKAGE DIMENSIONS (SOP32-P-525-1.27)

Units in mm

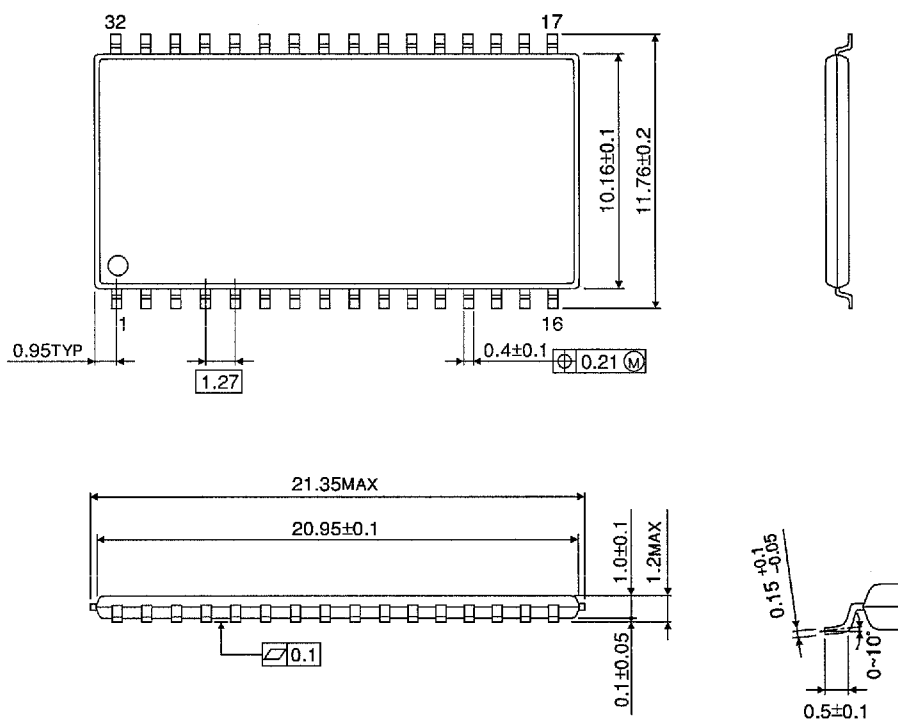


Weight: 1.10 g (typ)

TC51V8512AF - 12, - 15

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

Units in mm



Weight: 0.51 g (typ)

TC51V8512AFT-12, -15